RTL Verification Methodology and Closed Verification Solution for the PCIX Interface of the Atlantis Project

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Abstract

Integrated circuits present a large portion of the modern hi-tech industry. This industry characterized by intensive competition and increasing design complexity. The increase in design complexity causes an exponential increase in the complexity of the verification problem hence requiring the development of new tools and systems that are able to meet these new challenges.

A typical design spans a huge state space and the design can be in any point of this space at any time. An ideal verification system, would verify the design for each point in the state space. Clearly it is beyond a typical system's capability to simulate all scenarios due to limited time and computational resources.

In order to define a good verification system one should focus on several requirements:

- a system that is theoretically able to place the design in any state.
- a system able to gather information from all states visited.
- a system able to check the correct functionality of the design.
- a system able to achieve a predefined coverage of the state space in a given time using a given amount of resources.

In this project we present several possible solutions and evaluate the advantages and disadvantages of each. In addition, we defined a methodology for verifying a design of a PCIX interface. We carefully studied the protocol and the behavior of the design to be tested after which a detailed test plan was written.

The next stage involved the design and implementation of tools required by the complex verification process. These tools included a function library to support Galileo's HLVL in house language and checkers and trackers to monitor, steer and check the simulation process. A set of instructions was defined to easily allow a user to build an automatic test generator for his design. The new system was successfully integrated into Galileo's verification environment.