

Capacitive Sensing Project

Design of A Fully Differential Capacitive Sensing Circuit for MEMS Accelerometers

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Abstract:

MEMS (Micro Electro Mechanical Systems) accelerometers are becoming more and more commonplace as they offer a cheap and compact alternative to traditional accelerometers. One common and inexpensive measuring method is using a capacitive sensing circuit as the sensing element of the accelerometer. The design of such circuits is a highly challenging task due to the nature of MEMS accelerometers, which presents the analog designer with several problems. These include very low values of capacitors that need to be sensed and the large mismatch between them. Also, the typical MEMS sense capacitance is a few hundreds femtofarads, resulting in high sampling (KT/C) noise.

A possible solution to these problems is using a sensing circuit based on a fully differential cascode operational amplifier, and using a correlated double sampling (CDS) analog system as well as a very high oversampling rate to reduce the various measurement offsets and noises. The aim of this project was to design, simulate, implement and test this solution. This circuit will be fabricated using the CMOS AMI 1.6 micron technology, and then tested.

Typically, this analog circuit will be followed by an on-chip A/D converter, that is beyond the scope of this project.

Introduction:

Accelerometers are widely used in various applications ranging from navigation systems, monitoring mechanical systems and as an impact sensor for car air bag deployment.

The basic idea behind acceleration sensing is to measure the displacement of a proof mass suspended by a spring. This displacement is proportional to the acceleration exerted on the proof mass.

The capacitance based accelerometer uses plate capacitors to measure the deviation of the proof mass from its resting position. The mass is suspended by springs between two plates, creating two coupled plate capacitors between the mass and the plates.

For a single plate capacitor:

$$C_{total} = \frac{\epsilon_0 \epsilon_r A}{l + dl}, C_0 = \frac{\epsilon_0 \epsilon_r A}{l}, dC = C_{total} - C_0$$

Using the Taylor expansion for small displacements, dl can be approximated:

$$dl = \frac{-l^2}{\epsilon_0 \epsilon_r A} dC$$

where A is the overlapping area of the plates, l is the distance between the plates at

rest, ϵ_0 and ϵ_r are the electrostatic permittivity of vacuum and the relative permittivity of the insulator used between the plates, respectively.
Since all these parameters are known, dl can be calculated if dC is known.

Assuming the spring is in its linear region of operation:

$$dl = \frac{F}{K}$$

$$F = ma$$

Thus, the acceleration is:

$$\Rightarrow a = \frac{Kdl}{m} = \frac{K}{m} \frac{-l^2}{\epsilon_0 \epsilon_r A} dC$$

Where K is the spring constant and m is the mass of the proof mass.

It is thus possible to calculate the acceleration from the capacitance changes measured.

Challenges:

The MEMS accelerometer uses variable MEMS capacitors for the measurement. The capacitors and their springs are implemented on the same silicon die. Therefore, the capacitors are very small, approximately 1 picofarad with a few femtofarads of variable capacitance, and suffer from mismatches and parasitic capacitance. This causes several problems:

- The measured capacitance is very small, thus the sensitivity of the sensing circuit must be very high. This also causes the circuit to be susceptible to noises due to the small input signal.
- MEMS fabrication techniques suffer from limited accuracy which results in mismatch between the capacitances to be measured. This mismatch could result either in an offset to the input voltage or a random change in the circuit resolution, requiring software calibration.
- The measurement circuit should be able to operate at a switching frequency much greater than the maximal input signal frequency, to achieve a high oversampling rate. A high sampling rate eliminates the quantization noise typically introduced by A/D converters, and also assists in digitally attenuating thermal noise after the A/D conversion. Moreover, when the sampling frequency is much higher than the mechanical resonance frequency of the MEMS device, the effect of the measurement on the signal is negligible.

Fundamentals of capacitive sensing:

The basic capacitive sensing circuit consists of a differential operational amplifier (henceforth designated as “op-amp”) with a capacitive negative feedback loop.

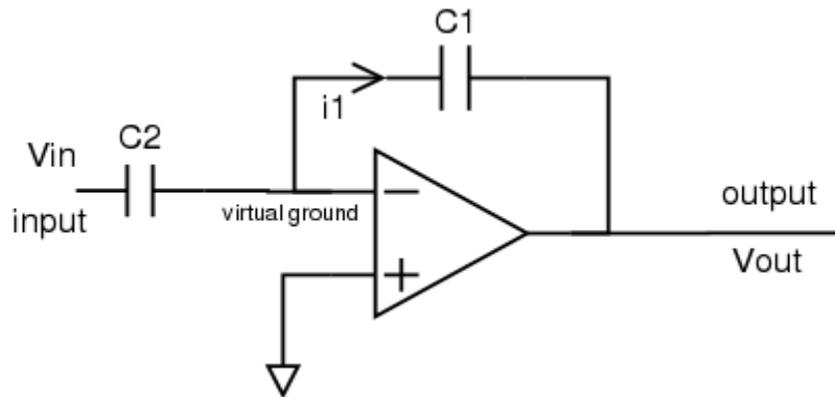


Fig 1 – Basic Capacity Sensor

In the small signal region of operation, the following analysis takes place:

$$i_1 = V_{in} \times SC_2 = -V_{out} \times SC_1$$

The gain of this circuit is $A = \frac{V_{out}}{V_{in}} = -\frac{C_2}{C_1}$

If either C1 or C2 is a variable capacitor, and the other is of a known and fixed size, it is possible to use this circuit to measure capacitance variations. This is done by driving pulses of charge through the circuit, and measuring the charge deposited on a capacitor connected to the output node.

Requirements:

- 8-bit sensing resolution – meaning that if the total input range is DV, and the total input attributed noise variance is dV, 256 different input values can be distinguished between at the output of the sensor. This could be mathematically expressed as $\log_2\left(\frac{DV}{dV}\right) \geq 8$. That is, if an A/D converter was connected to the circuit, it would be possible to operate it with 8-bit resolution.
- 100 KHz sampling rate - In order to achieve the oversampling mentioned earlier.
- In order for the amplifier to be an operational amplifier, it must have at least 70 dB differential gain.
- Maximal power consumption 50 mW.

Implementation:

First, a fully differential cascode operational amplifier was studied and implemented. In order to maximize its performance, a small signal model was developed and simulated using Matlab and Mathematica. Using the guidelines attained by these simulations, the amplifier was implemented in Cadence, and further simulated using the Cadence SPICE simulator. The SPICE simulations gives the designer a good estimation of the circuit's performance and behavior. The design was modified until it fulfilled all the requirements.

In order to avoid floating node issues, attenuate correlated noises and eliminate various input and amplifier offsets, a CDS (Correlated Double Sampling) system was studied and implemented.

CDS is a technique used to cancel offsets by sampling the signal twice. The input signal to the circuit is modulated in two phases. In the first phase V_{in} is positive, and in the second, V_{in} is negative. The offset, however, is the same in both cases. CDS only eliminates offsets that can be expressed as an input error voltage.

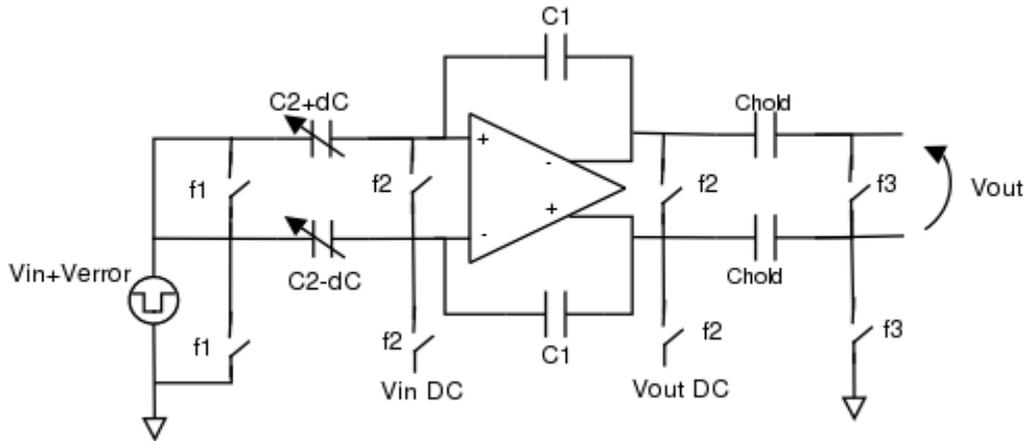


Fig. 2 – A fully differential amplifier with CDS

CDS uses four clock phases to sample and integrate the input signal twice. In each sample the input voltage has opposite signs, but the offset voltage has the same polarity. The integration results are then stored on the hold capacitors. Thus, when the results are subtracted at the output, the offsets are canceled out.

Once the circuit was designed, simulated and optimized, the schematic had to be transformed into a layout that can be sent to fabrication. Although automatic layout synthesizers exist, the layout they produce is not satisfactory for analog designs. When designing the layout manually, better symmetry can be achieved, leading to lower mismatches. Mismatches between transistors, capacitors or even wires degrade the performance of the circuit and cause offsets.

Wire matching is achieved by routing wires to be of the same length and material, while insuring their environment (e.g. electrical boundary conditions) is as similar as possible. Component matching (e.g. Transistors, resistors and capacitors) is achieved by dividing each component into an even number of identical blocks, and using the common centroid technique. That is, if two (or more) components are to be matched, their blocks are placed in a checkerboard like pattern, to achieve symmetry between them.

Where applicable, a novel matching technique [7], which promises a great improvement in matching over the common centroid technique, was used.

Conclusions:

A capacitive sensing circuit was studied, designed, optimized and implemented. It meets the requirements, and serves as a prototype of a sensor that can be integrated with the MEMS accelerometer on a single chip.

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Bibliography:

1. CMOS analog circuit design / Phillip E. Allen, Douglas R. Holberg, 2nd ed., Oxford University Press, 2002
2. A Three-Axis Micromachined Accelerometer with a CMOS Position-Sense Interface and Digital Offset-Trim Electronics / Mark Lemkin and Bernhard E. Boser, IEEE Journal of Solid-State Circuits, Vol. 34, No. 4, Page 456, April, 1999.
3. A Micromachined Fully Differential Lateral Accelerometer / Mark Lemkin and Bernhard E. Boser, IEEE 1996 Custom Integrated Circuits Conference, Page 315.
4. Design and Simulation of A CMOS-MEMS Accelerometer / Gang Zhang , Project Report, Carnegie Mellon University, May 1998.
5. Optimal Vdsat for Folded Cascode Amplifier / Circuit Sage Website.
6. Offset cancellation lecture slides / V. Petkov, Analog integrated circuits course, Berkley university
7. A New Current Mirror Layout Technique for Improved Matching Characteristics / Mao-Feng Lan, Anilkumar Tammineedi, Randall Geiger, Department of Electrical and Computer Engineering, Iowa State University, U.S.A.
8. Analysis of 1/f Noise in CMOS APS / Hui Tian, Abbas El Gamal, Information Systems Laboratory, Stanford University, U.S.A.