Network Controller for High QoS

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Abstract

This project demonstrates the benefits and architecture of a hardware accelerated Quality-of-Service (QoS) connection routing and establishment system. The project is based on a constrained flooding QoS route searching algorithm that is optimized in terms of connection setup, success percentile, connection establishment time and consumption of network resources.

The main idea in this approach is the aggregation of the three parts of a QoS system: connection establishment signaling, connection routing and connection admission control into a single low cost hardware supported protocol and mechanism.

Hardware based architecture is presented that effectively implements all the components of the proposed mechanism. The architecture does not attempt to replace the existing router architectures. It assumes generalized router architecture and proposes to add new units that will implement the algorithm. Such a hardware based solution can easily scale to support the per flow connection setup demands of large service provider or enterprise networks.

Introduction

Modern IP networks are required to provide Quality of Service (QoS) guarantees to individual end-to-end connections. QoS is the probability of the network meeting a given traffic contract. Without QoS the network could not provide a good solution for real time applications such as video conference or remote surgery, due to the loss of an unlimited amount of packets, out of order packet arrival and variation in rate of arrival depending on the load of the system. Establishment and maintenance of QoS connections is one of the most active research areas in the field of converged packet-switching networks.

The Ellipse Algorithm

Professor Israel Zidon and Nitzan Miron [1] proposed a solution for the QoS problem. A restricted flooding algorithm to reserve bandwidth that executes in a distributed manner to find a path between source and destination nodes in a network that meets the QoS requirements (bandwidth and max hop count). The proposed algorithm, called Ellipse, is a dynamic resource reservation based solution that can easily scale to support the individual connection setup demand of a large service provider or enterprise network. It is distributed among all the routers (NIMs) that connect a sub-network to the global network.

A typical QoS reservation mechanism is composed of three essential components: QoS based routing, resource reservation signaling and admission control. These components have often been addressed separately in the past but their implementations were never integrated. The Ellipse algorithm provides an integrated solution for the three components.

The algorithm performs constrained flooding to find the desired path. Upon source request, it tries to dynamically allocate network resources in order to meet the QoS requirements. Initially the application sends to the adjacent router (source node) a connection request with the following information:

- Required bandwidth
- Maximum allowed connection hop-count
- Connection identifier
- Destination node identifier

The source node forwards the message to all its neighbors. Upon receiving the least hop-count probe all intermediates nodes perform the following task. If enough bandwidth is available for reservation on the outgoing link and there is a feasible route through the neighbor that satisfies the maximum hop-count restriction and the route is loop-free, the node reserves the required resources and forwards the updated *probes* over all the eligible links. A node responds with a reject message if it has no eligible links, or if it receives rejects messages for each *probe* it has sent, or at least one of the previously received *probes* has smaller or equal hop-count. The destination node answers with an *accept* message to the first *probe* it receives.

Architecture and Design

The network controller for high QoS project involved the design, implementation and simulation of VLSI architecture for the Ellipse algorithm. The hardware solution overcomes many of the scalability and deployment barriers present in other solutions. The architecture effectively implements all the components of the proposed mechanism**.** It assumes generalized router architecture and proposes adding additional units that implement the algorithm.

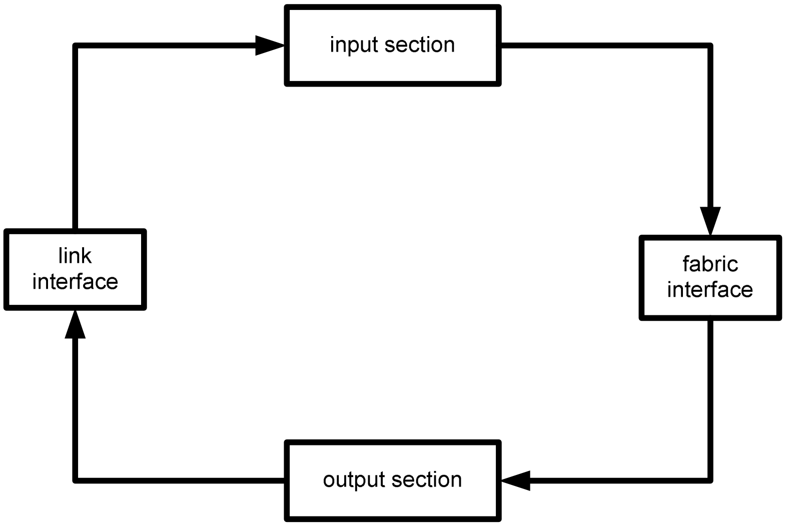


Fig 1 : Generalized router architecture (NIM)

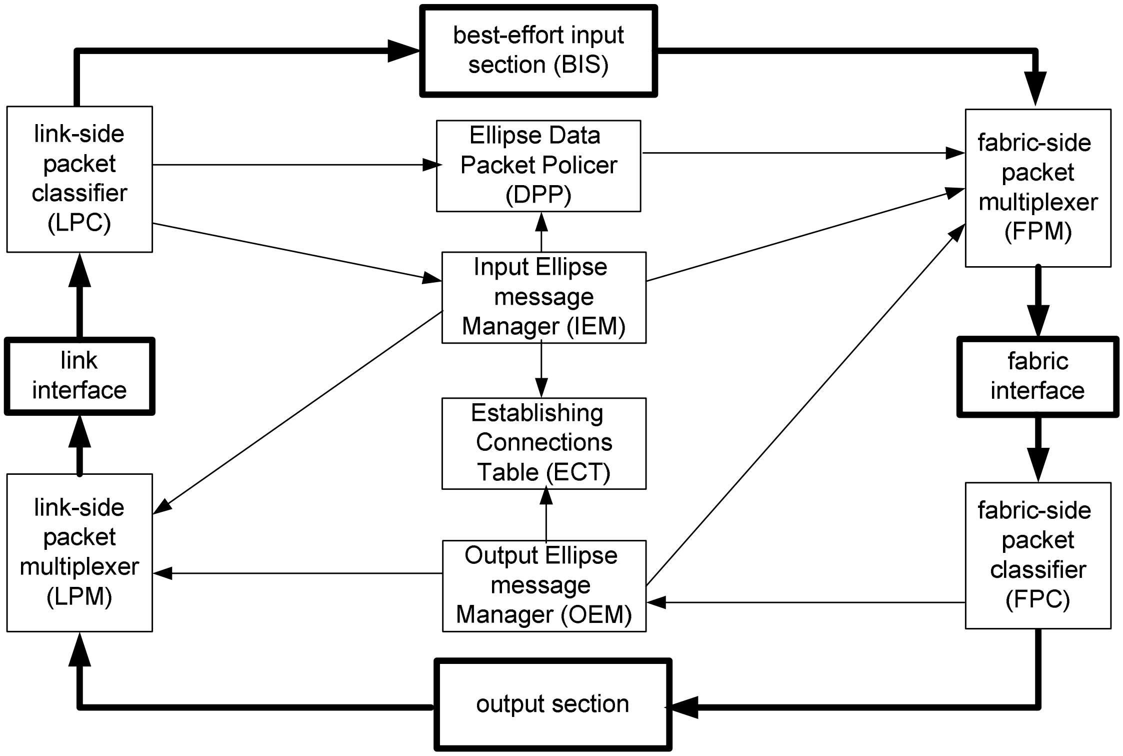

best-effort input section (BIS)
link-side packet classifier (LPC)
Ellipse Data Packet Policer (DPP)
fabric-side packet multiplexer (FPM)
Input Ellipse message Manager (IEM)
link interface
fabric interface
Establishing Connections Table (ECT)
link-side packet multiplexer (LPM)
Output Ellipse message Manager (OEM)
fabric-side packet classifier (FPC)
output section

Fig 2 : A router (NIM) with extension for Ellipse algorithm

Packet Classifiers

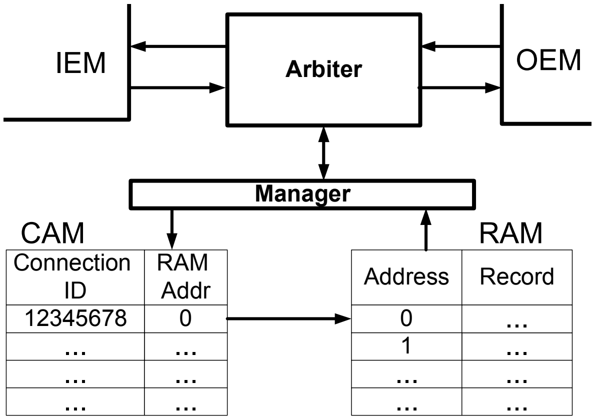
There are two packet classifiers per NIM, the LPC and the FPC. The packet classifiers classify the incoming packets and forward them to the appropriate units. Control messages from the link are forwarded to the IEM while data messages are forwarded to BIS and DPP. Control messages from fabric forwarded to OEM while data messages forwarded to output section.

Packet Multiplexers

There are two packet multiplexers per NIM, the LPM and the FPM. The packet multiplexers, multiplex incoming packets from four inputs (IEM, OEM, DPP, BIS), and forward them to the appropriate units. The packet multiplexers perform smart arbitration to determine which packet is to be forwarded to the output interface (link / fabric). A QoS message always will be given a priority over other messages.

ECT (Data Base)

The ECT is a shared database between the IEM and OEM of a same NIM. The ECT stores information regarding the QoS link and its host NIM. The ECT was implemented using routing table structure, and is a specially designed content addressable memory that enabled performing a search for a record in $O(1)$ time. The ECT memory size is proportional to the network size.



Connection ID	RAM Addr
12345678	0
...	...
...	...
...	...

Address	Record
0	...
1	...
...	...
...	...

Fig 3 : The ECT Architecture

Message Managers

There are two message managers per NIM, the IEM and the OEM. The message managers are the hardware implementation of the high level Ellipse algorithm. The message managers are the most complex, sophisticated and interesting blocks in the design. The message managers process Ellipse control messages and make decisions regarding QoS connections establishment.

Testing and Simulation

The Ellipse algorithm is a very complex algorithm, and for every input to the algorithm there are many possible outputs, as the output is dependent on the scenario and on the network architecture. Therefore a test plan had to be carefully designed taking into consideration that the tested NIM is a part of a node and the node is a part of a bigger network. The test plan included white box testing, carefully selecting scenarios for complete code coverage, black box testing and using processes that represent different NIM's that operates together.

Project Challenges

This project included the hardware design and implementation of a high level distributed algorithm that was specified as pseudo code. This type of work required a deep understanding the QoS problem and the given solution. The given algorithm needed to be further distributed so that it could run at different locations in parallel on the same network node.

In order to be able to execute, the algorithm requires memory to store data in each node. A combination of CAM and RAM memory was used to efficiently store and retrieve data.

The distribution of the solution in the network node and between different nodes required synchronization mechanisms. The synchronization task was rather complex and required a lot of design effort.

Verifying the correct functionality of the design was far from trivial. The test plan included several simulation techniques such as black box testing, white box testing and code coverage testing.

Conclusions

Completing the design required the use several disciplines, from high level software methodologies to low level logic design methodologies. The results show that the solution provided by Zidon/Miron [1] for the quality of service problem can be implemented efficiently in hardware with minimal changes to existing routers. Previous studies show that this is currently one of the most efficient solutions to the QoS problem.

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References

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[2] VHDL Programming - Douglas L.Perry

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