Analysis of Memristor Based Circuits

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Introduction : The Missing Fundamental Element

We all familiar with basic electronic elements: the resistor, the capacitor and the inductor. In 1971 professor Leon Chua from UC Berkeley reasoned by arguments of symmetry, that there should be a fourth fundamental element, which he called a memristor. He predicted its behavior to be a relation between φ (magnetic field) and q (charge) on it as follows:

$$d\varphi = M \cdot dq$$

By simple mathematical manipulation the following expression is obtained:

$$\frac{v(t)}{i(t)} = M(q(t))$$

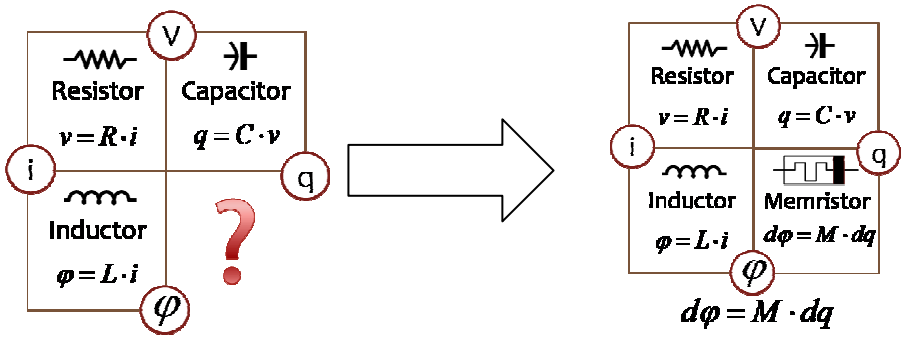


Fig 1 : The Missing Fundamental Element

Therefore, it can be said that a Memristance "*M*" as defined by Prof. Chua is actually a resistance that is dependent on the history of the charge that has passed through it.

Despite the simplicity and the soundness of the symmetry argument that predicts the existence of the fourth ideal element, experimental realization of a quasi-ideal memristor, defined by the single-valued relationship $d\varphi = M \cdot dq$ remained elusive. Until 2008 no one had presented either a useful physical model or an example of a memristor. In May 2008 a team from HP announced that they had succeeded in producing a device, based on electrical switching in thin-film devices, with behavior similar to Prof Chua's predicted memristor.

Future Potential of the Memristor

The memristor is a most promising device with the potential of bringing significant changes in the field of micro and nano-electronic devices. It is predicted that future applications will include non-volatile memories with multiple TeraBytes in an area of 1 cm^2 effectively reducing computer bootstrap time to zero, memories 10^6 times faster than magnetic disks with a much lower power consumption, implementation of logic gates inside the memory effectively requiring zero area, implementation of fast non-linear devices for enabling brain emulation (synapses) and many more.

Project Goals

As no device or behavioral model for the memristor is publicly available to memristor circuit designers, the first goal of the project was to develop an accurate behavioral VerilogA model of the memristor to allow simulation of memristor based circuits. In order to gain a deeper insight and understanding of the behavior of parallel/series memristor circuits and of different MC and ML configurations (circuits containing a memristor and a capacitor or an inductor), a complete mathematical analysis of each configuration was performed. Once these basic building blocks were developed, the next goal was to design and implement a complete memristor memory array. This included a read and write module specifically designed for a memristor-based random access memory cells. This unique module overcomes most of the main problems of this type of memory implementation. The final goal of the project involved the implementation of FPGA programming switches and combinational logic gates based on memristor devices.

Behavioral Memristor Model

Memristor models were developed in two stages using the VerilogA language and the Cadence analog circuit simulation environment. Initially a linear model was developed. This model was based on Prof. Chua's theoretical equations (1) and additional electrical characteristics of the device published by HP labs [1].

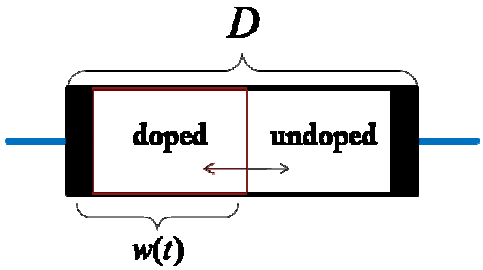


Fig 2 : Memristor Basic Structure

$$v(t) = \underbrace{\left[R_{ON} \frac{w(t)}{D} + R_{OFF} \left(1 - \frac{w(t)}{D} \right) \right]}_{R} i(t) \qquad ; \qquad \frac{dw}{dt} = \mu_V \frac{R_{ON}}{D} i(t) \qquad (1)$$

There were several practical issues that had to be overcome. The fact that a real device has finite dimensions required the definition of a limiting window function. This issue was further complicated as experimental evidence showed that the electrical behavior of the device was different at the edges. Therefore several variations of the window function had to be investigated. Next a more accurate non-linear model was developed. More recent publications reported non-linear dependency of the state variable w(t) on the current i(t), where the current direction also affects the behavior of w(t), and the existence of an effective current threshold. The non-linear VerilogA model that was developed in this project was based on a mathematical model developed by Shahar Kvatinsky et.al. accounted for this newly reported behavior. This included the use of Kvatinsky's mathematical approximation (2) instead of the complex expression published in [2]:

$$\frac{dx(t)}{dt} = \begin{cases} k_{off} \left(i(t) - i_{off} \right)^{\alpha_{off}} f_{off}(x), & 0 < i_{off} < i \\ k_{on} \left(i_{on} - i(t) \right)^{\alpha_{on}} f_{on}(x), & i < i_{on} < 0 \\ 0, & Otherwise \end{cases} \qquad (2)$$

and also included the modeling of the continuous doped area width variation (3):

$$w(t) = \int_0^t \left(\mathbb{I}_{on}(i) \cdot k_{off} \left(i(t) - i_{off} \right)^{\alpha_{off}} \cdot W(i,w) + \mathbb{I}_{off}(i) \cdot k_{on} \left(i_{on} - i(t) \right)^{\alpha_{on}} \cdot W(i,w) \right) dt \qquad (3)$$

Creating a stable model also required extensive knowledge of the analog hardware description programming and the correct analysis of CAD tools simulations results. From the simulation of this model, the typical memristor I-V hysteresis characteristic shown in Fig. 3 was obtained.

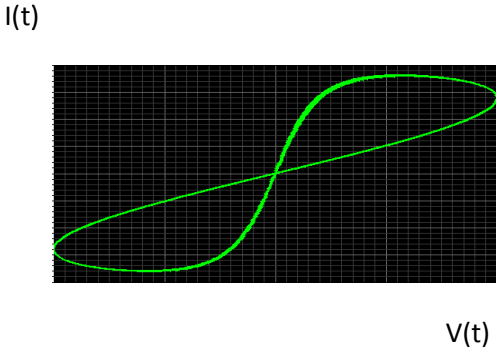


Fig 3 : Memristor Hysteresis Characteristic

Theoretical Analysis of MC and ML Circuits

As stated above, the next task was to gain a deeper insight and understanding of the behavior of different basic MC and ML circuits. A complete mathematical analysis of each circuit was performed. For MC circuits, the analysis led to an ODE of the following type (4):

$$\frac{dq}{dt} = -\frac{q(t)}{A + Bq(t)} \qquad (4)$$

which was solved with the help of the Lambert function: $z = W(z)e^{W(z)}$
The behavior is summarized in Fig 4.

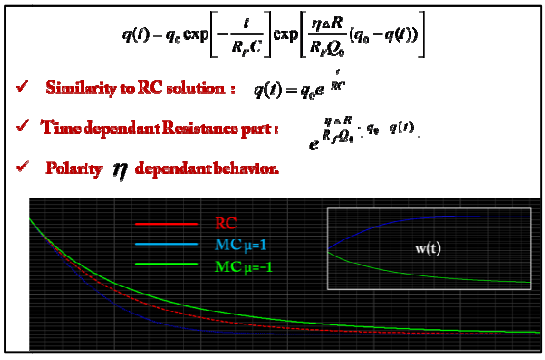


Fig 4 : Step response of an MC Circuit

For the case of ML circuits, an ODE of the type (5) had to be solved and the behavior is summarized in Fig 5.

$$L\frac{d^2q}{dt^2} + R_O\frac{dq}{dt} - \eta\frac{\Delta Rq}{Q_O} \cdot \frac{dq}{dt} = 0 \qquad (5)$$

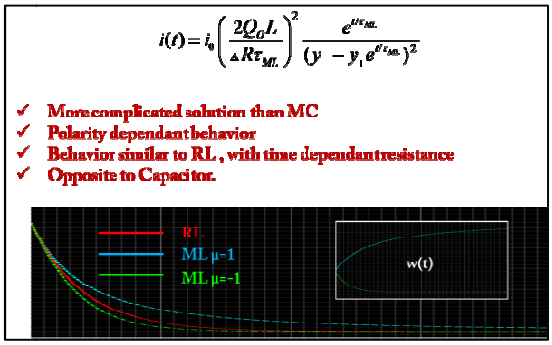


Fig 5 : Step response of an ML Circuit

MLC circuits were also investigated and the step response is shown in Fig. 6. However, the complex theoretical analysis was beyond the scope of this work.

I(t)

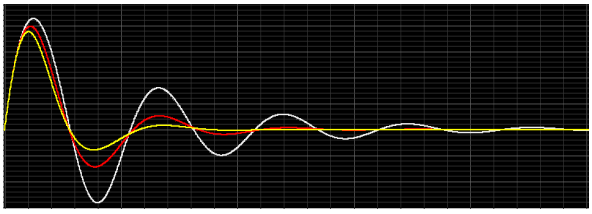


Fig 6 : Step response an MLC Circuit

Memristor-based Memory

The memristor (as can be deduced from its name), is capable of memorizing its own resistance. Different resistance values can be used to represent different values of data. There are many significant advantages of using this device to store data. These include, extremely small area (compared to an SRAM cell), no leakage, CMOS compatibility, excellent power efficiency and non-volatility.

The basic and most intuitive implementation of memory with memristors is RRAM (Resistive Random Access Memory). Using one memristor it is possible to implement a DRAM like memory cell. Initially, the resistance is set by the passage of a well-defined current through the device. Once the current ceases, it will retain its resistance indefinitely even if the power is cut off. There is no need to refresh it (as a result of leakage) as the information is stored as resistance, unlike DRAM, which stores the data as an electric charge. When power is restored the device will have the same resistance as it had before the power was disconnected. Defining low resistance to represent logic '1' and high resistance to represent logic '0', it is possible to store binary data and read it at a later stage. A complete memory array could be built from memristors with all the advantages stated above. The part of the project also included a unique implementation of a read/write mechanism for storing one bit of data based in a memristor memory cell. A redundancy feature was added, which always ensures that the data is read or written correctly and that the action is performed at high speed. This design overcomes the main problem of the memristive memory refresh requirement due to the destructive nature of multiple read operations. Schematics and timing diagrams of the memory are shown in Figs. 7 and 8.

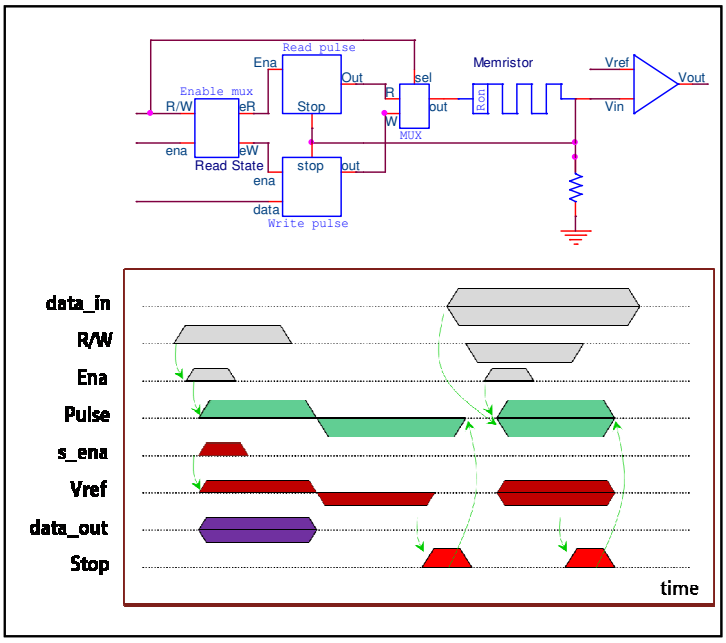


Fig 7 : R/W Mechanism and Timing Diagram

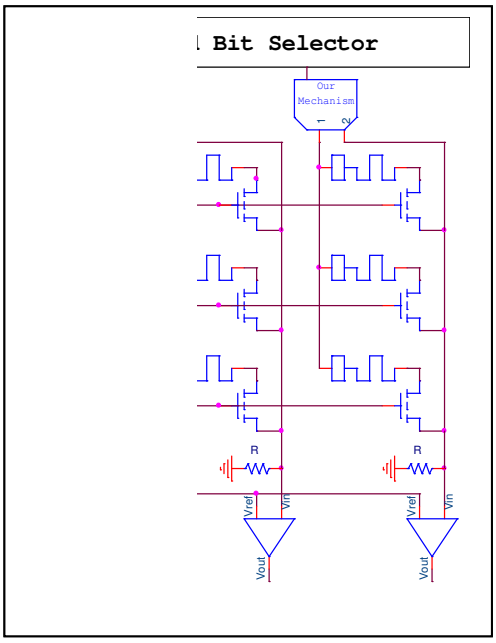


Fig. 8 : Structure of RRAM Array Using our unique mechanism

Memristor-based Logic Circuits

In the final part of the project it was shown how memristors can be used for the implementation of logic blocks which would enable the implementation of a complete computer. One approach would be to use it as FPGA configurable switches instead of the transfer gates used today. Several memristor-switch configurations were designed and simulated. These implementations can potentially save die area and thus will also reduce power consumption.

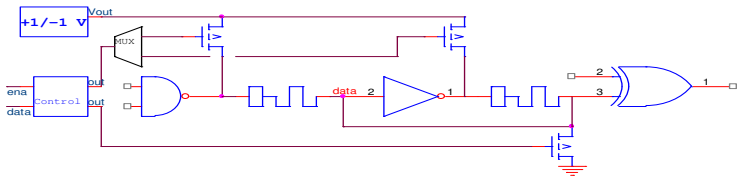
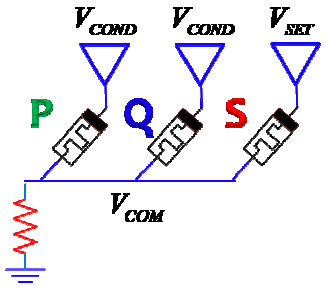


Fig. 9 : FPGA memristor switch implementation

In the proposed FPGA configuration shown in Fig. 9 a +1/-1V voltage source is required. The design uses only one grounding transistor for many memristor switches and therefore approx. only one transistor is needed for each switch.

The second approach is to implement logic gates using device resistance as data input/output. Using the IMPLY operation and constant zero (Fig. 10), basic combinational logic gates such as NAND, AND, NOT, OR, NOR were built and the advantages and disadvantages of such implementations were evaluated.



p	q	s	p,q→s
0	0	0	1
0	1	0	1
1	0	0	1
1	1	0	0

Fig. 10 : Memristor-based NAND gate

Conclusions

VerilogA memristor models were developed based on the work done at HP and by S. Kvatinsky. Extensive analysis of basic memristor configurations including MC and ML circuits was performed and compared with simulations using these models. An efficient design of memristor-based memory was implemented including a unique R/W Module. In addition, a method was proposed to implement multiple reconfigurable FPGA switches based on memristor resistance. Also, it was shown how the memristor can be easily used to implement a complete logic basis.

One of the main challenges of this project included overcoming the lack of literature and information on this novel fundamental electric element. Other difficulties included broadening of mathematical knowledge to cope with the complex theoretical analysis of the memristor circuits. Several configurations were designed and simulated in order to develop efficient implementations for the different circuits presented in this work.

Note : This project is a part of a memristor research project being performed by our supervisor Shahar Kvatinsky, led by Prof. Avinoam Kolodny, Prof. Uri Weiser and Prof. Eby Friedman (Rochester University, New York).

References:

[1] “The missing memristor found”. Dmitri B.Strukov & HP team

[2] “Switching dynamics in titanium dioxide Memristive devices”. Dmitri B.Strukov & HP team

[3] “Memristor-The missing circuit element”. Leon O.Chua.

[4] “The elusive memristor: properties of basic electrical circuits”. Yogesh N Joglekar, Stephen J.Wolf

[5] “Memristive switches enable ‘stateful’ logic operations via material implication”. Julien Borghetti, Gregory S. Snider et.al.