

A 10-bit 1Gsamples/sec Current-Steering D/A Converter Rad-Hard by Design

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Abstract

High speed Digital to Analog converters (DACs) are essential components of a large number of modern electronic systems, providing the necessary conversion of signals encoding information in bits to signals encoding information in their amplitude. In general, they are parts of a larger system, such as wired and wireless transmitters, arbitrary waveform generators and local oscillators. Another application that requires fast DACs is direct digital synthesis (DDS), which is a method of producing an analog waveform by generating a time-varying signal in digital form and then performing a digital-to-analog conversion. The goal of this project was to design a high speed DAC for DDS capable of working in environments with high levels of ionizing radiation, namely in outer space.

The market for radiation tolerant devices is small, and thus most commercial manufactures of integrated circuits have been reluctant to invest in this area. In this project, radiation tolerance is achieved by circuit and layout techniques i.e. Rad Hard by Design (RHBD), instead of the more common technique of using special CMOS fabrication processes. This RHBD methodology achieves radiation tolerance using standard CMOS technology thus drastically lowering the cost of the device.

One of the challenges faced in the project was to combine high speed and high resolution requirements of the converter with RHBD methodology. Since this methodology dictates the use of PMOS transistors, (or NMOS circular transistors with large gate area), the resulting circuits have relatively large capacitances which reduce the operating frequency. Therefore, this project proposes a non-conventional design that would generally be an unnatural choice for DACs.

For high speed and high resolution DACs, the current steering architecture is preferable since it can drive a resistive load directly without the need for voltage buffers. Current-steering DACs are based on an array of matched current sources which are unity decoded or binary weighted. Unity decoded current sources allow reduction in the glitch energy and differential nonlinearity (DNL). However, they cause an increase in the overall layout area and the decoding logic complexity, which limits the speed of the converter. On the other hand using of binary weighted current sources does not require any decoding logic, introducing high DNL and an increase in glitch energy. In the designed DAC a combination of the two methods was used to meet the high performance requirements.

In the first part of the project, extensive circuit simulations were performed as well as optimization of the circuit in terms of glitch energy, INL and DNL reduction. In order to ensure temperature robustness, a feedback circuit was developed. In the second part of the project, the layout of the circuit was implemented in accordance with the RHBD methodology.

This project presents a 1GS/s 10-bit CMOS DAC designed with a RHBD current steering segmented architecture with the 6 LSB bits being binary weighted and 4 MSB bits unary weighted. The achieved INL is better than 0.3 LSB and DNL less than $1.8e-3$. At a conversion rate of 1 GS/s, the power consumption is 30 mW. High tolerance to temperature variation has been achieved using a feedback circuit. The chip was designed and implemented in a standard 0.13 μ m CMOS Tower technology and has an area of 0.125 mm².

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