**Project Name**

**Students :**
**Supervisor :**
**Semester :** Aviv 2015

**Project Description :**
Modern flash-based solid-state drives contain aggressive 19nm scaling of floating-gate transistors. As a result, data is often stored with errors due to inter-cell interference, coupling, random-telegraph noise and more. The signal-to-noise ratio becomes even worse as density increases. In order to provide reliable data storage, system controller employs error-correcting algorithms.

The goal of this project is to design and implement an advanced error-correction soft-decision Reed-Solomon encoder and decoder.

**Project Requirements:**

- Pipelined architecture
- Minimal on chip memory
- Real time performance
- Maximum area efficiency
- Synthesis
- Physical design (layout)

**Project Specifications:**

- Clock Frequency : 150 MHz
- Area : 5x5 sq. mm
- Maximum number of IOs : 120
- Technology : Tower 0.18u CMOS

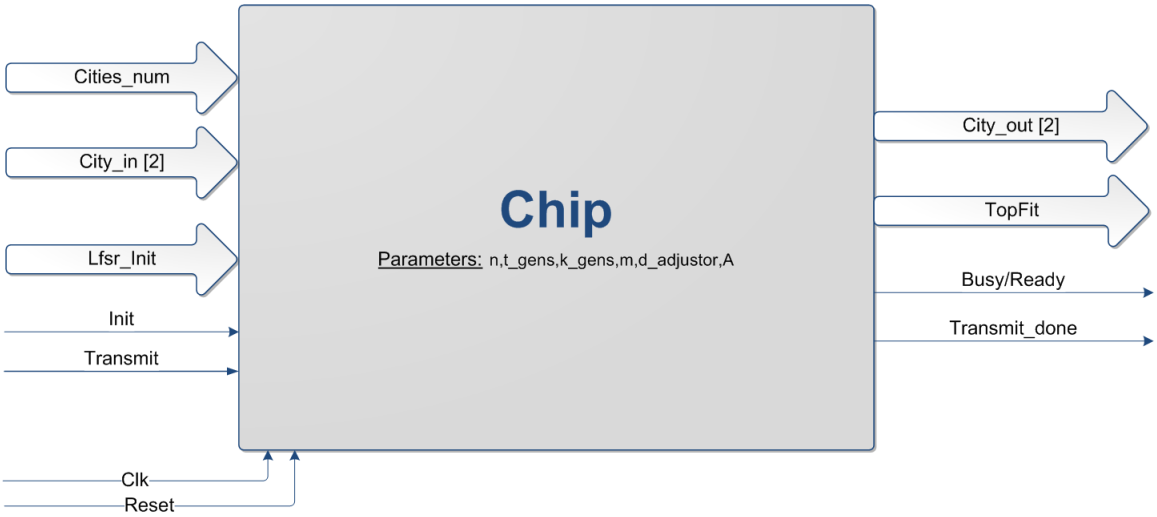
| Development Stages / Design Flow | Tools |
|---|---|
| Software Simulation | C/Matlab |
| Architectural and Logic Design | |
| HDL Implementation | VHDL/Verilog |
| Functional simulation | Ncsim/VCS |
| Synthesis | Design Compiler |
| Layout Design | First Encounter |

## Literature

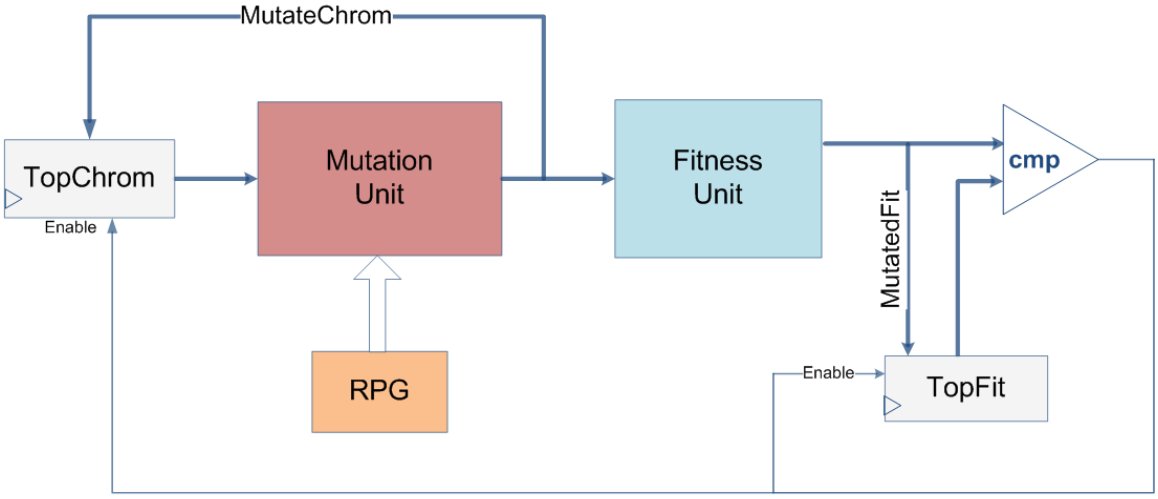
## Alternative solutions

## Selected solution

## Top Level Interface




## Top Level Architecture



| **Provisional/Preliminary Schedule** | **Week** |
|---|---|
| Task A | 1-3 |
| Task B | 3-5 |
| Task C | 6-9 |
| Task D | 9-12 |
| Task E | 13 |
| Task F | 14 |

Please prepare a Gantt chart as follows: Gantt Chart Example: